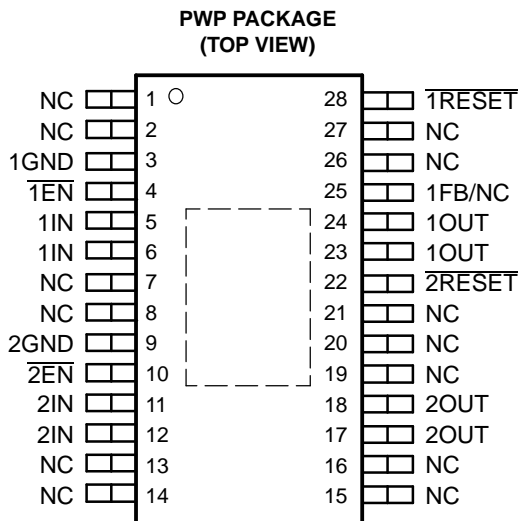


## FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **Dual Output Voltages for Split-Supply Applications**
- **Output Current Range of 0 mA to 1.0 A Per Regulator**
- **3.3-V/Adjustable Output**
- **Fast Transient Response**
- **3% Tolerance Over Load and Temperature**
- **Dropout Voltage Typically 350 mV at 1 A**
- **Ultra-Low 85- $\mu$ A Typical Quiescent Current**
- **1- $\mu$ A Quiescent Current During Shutdown**
- **Dual Open-Drain Power-On Reset With 200-ms Delay for Each Regulator**
- **28-Pin PowerPAD™ TSSOP Package**
- **Thermal Shutdown Protection for Each Regulator**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



NC – No internal connection

## DESCRIPTION/ORDERING INFORMATION

The TPS767D301-EP dual-voltage regulator offers fast transient response, low dropout (LDO) voltages, and dual outputs in a compact package and incorporates stability with 10- $\mu$ F low-ESR output capacitors.

The TPS767D301-EP dual-voltage regulator is designed primarily for DSP applications. This device can be used in any mixed-output voltage application, with each regulator supporting up to 1 A. Dual active-low reset (RESET) signals allow resetting of core logic and I/O separately.

### ORDERING INFORMATION

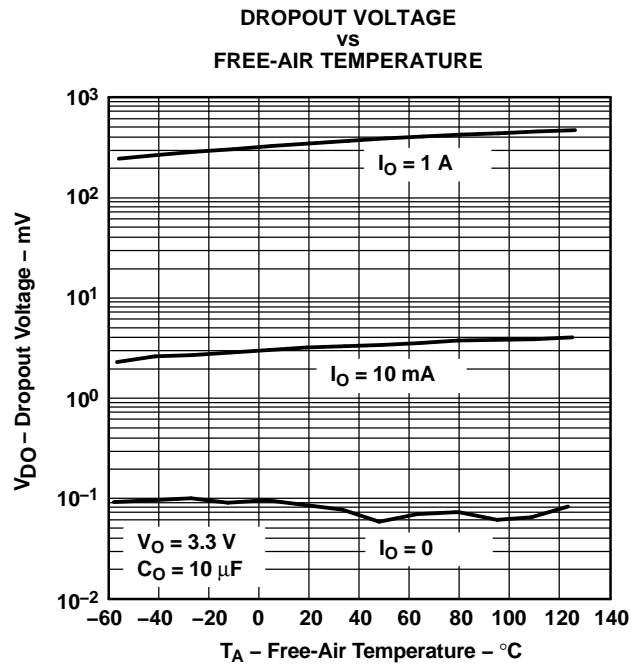
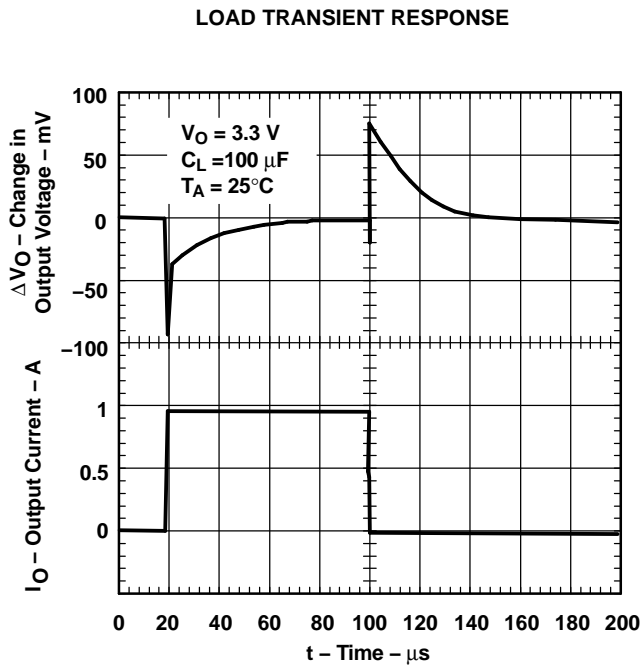
| $T_J$          | REGULATOR 1<br>$V_O$        | REGULATOR 2<br>$V_O$ | TSSOP (PWP)       |
|----------------|-----------------------------|----------------------|-------------------|
| –55°C to 125°C | Adjustable (1.5 V to 5.5 V) | 3.3 V                | TPS767D301MPWPREP |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)



Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85  $\mu$ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO device also features a sleep mode; applying a TTL high signal to enable ( $\overline{EN}$ ) shuts down the regulator, reducing the quiescent current to 1  $\mu$ A at  $T_J = 25^\circ$  C.

The  $\overline{RESET}$  output of the TPS767D301-EP initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767D301-EP monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767D301-EP is offered in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS767D301-EP is available in a 28-pin PWP (TSSOP) package. The device operates over a junction temperature range of  $-55^\circ$  C to  $125^\circ$  C.

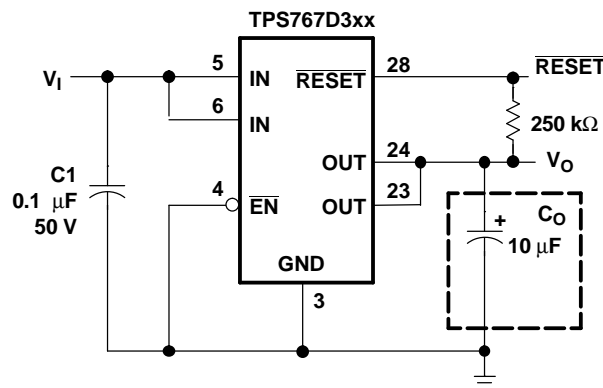
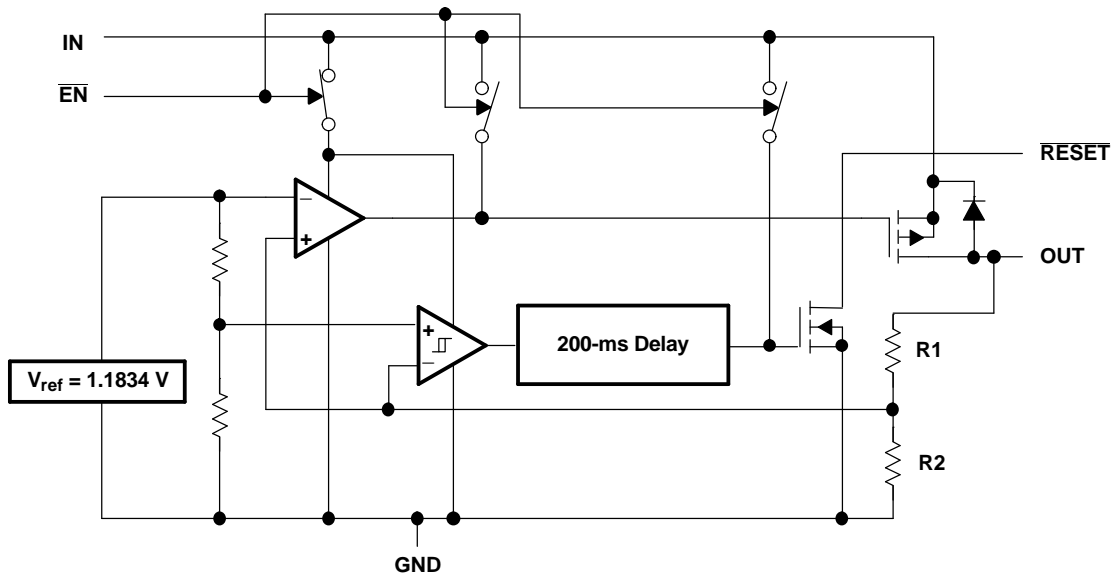
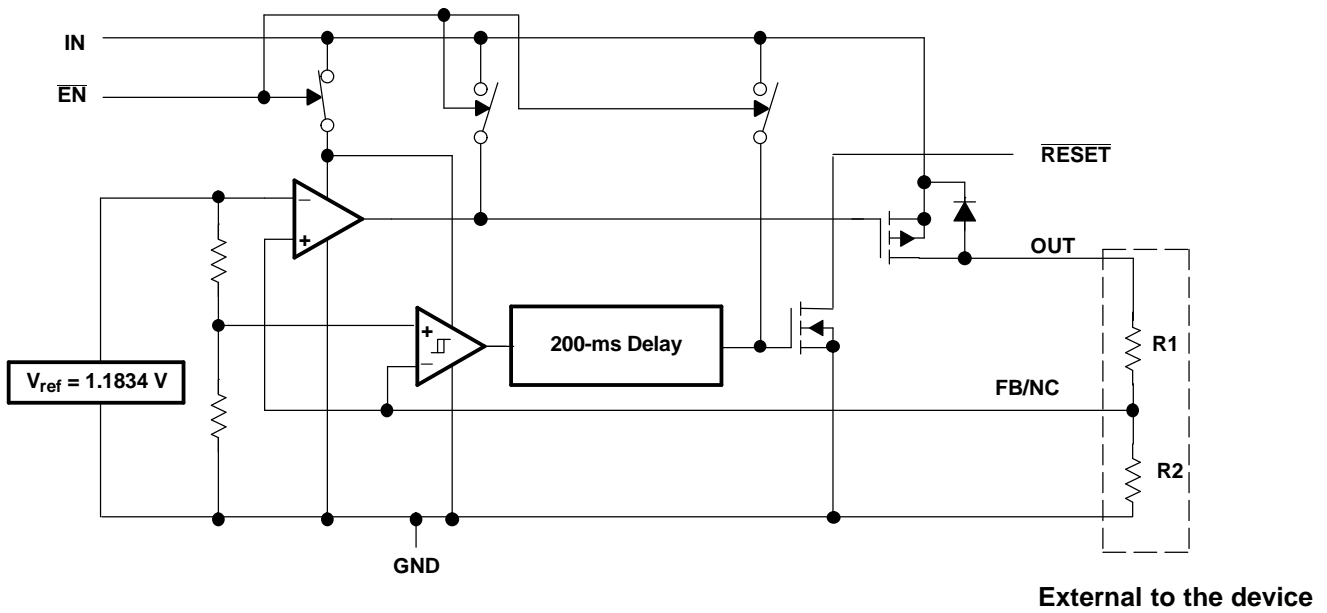


Figure 1. Typical Application Circuit (Fixed Versions) for Single Channel

**FUNCTIONAL BLOCK DIAGRAM**  
 Adjustable Version (for Each LDO)



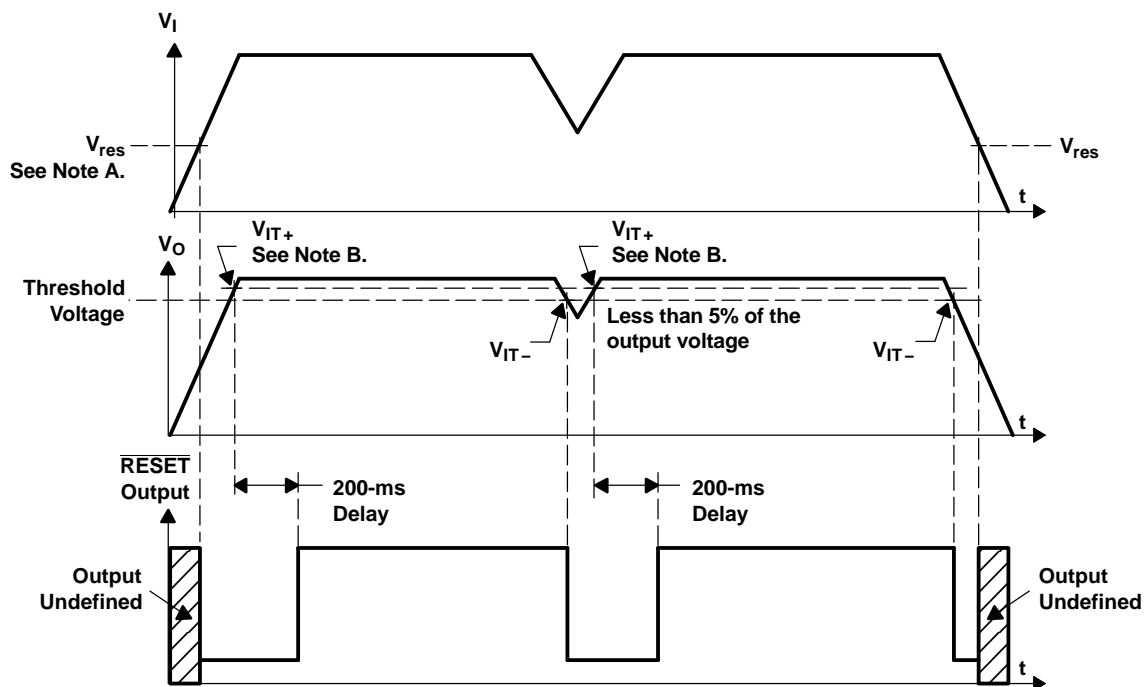
**FUNCTIONAL BLOCK DIAGRAM**  
 Fixed-Voltage Version (for Each LDO)



TERMINAL FUNCTIONS

| TERMINAL            |                                  | I/O | DESCRIPTION                                                                                        |
|---------------------|----------------------------------|-----|----------------------------------------------------------------------------------------------------|
| NAME                | NO.                              |     |                                                                                                    |
| 1GND                | 3                                |     | Regulator 1 ground                                                                                 |
| $\overline{1EN}$    | 4                                | I   | Regulator 1 enable                                                                                 |
| 1IN                 | 5, 6                             | I   | Regulator 1 input supply voltage                                                                   |
| 2GND                | 9                                |     | Regulator 2 ground                                                                                 |
| $\overline{2EN}$    | 10                               | I   | Regulator 2 enable                                                                                 |
| 2IN                 | 11, 12                           | I   | Regulator 2 input supply voltage                                                                   |
| 2OUT                | 17, 18                           | O   | Regulator 2 output voltage                                                                         |
| $\overline{2RESET}$ | 22                               | O   | Regulator 2 reset                                                                                  |
| 1OUT                | 23, 24                           | O   | Regulator 1 output voltage                                                                         |
| 1FB/NC              | 25                               | I   | Regulator 1 output voltage feedback for adjustable version and no connect for fixed-output version |
| $\overline{1RESET}$ | 28                               | O   | Regulator 1 reset                                                                                  |
| NC                  | 1, 2, 7, 8, 13–16, 19–21, 26, 27 |     | No connection                                                                                      |

TIMING DIAGRAM



- A.  $V_{res}$  is the minimum input voltage for a valid  $\overline{RESET}$ . The symbol  $V_{res}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.
- B.  $V_{IT-}$  – Trip voltage typically is 5% lower than the output voltage ( $95\% V_O$ ).

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                    |                                              |                           | MIN                          | MAX                  | UNIT |
|------------------------------------|----------------------------------------------|---------------------------|------------------------------|----------------------|------|
| V <sub>I</sub>                     | Input voltage range <sup>(2)</sup>           |                           | -0.3                         | 13.5                 | V    |
| V <sub>I</sub>                     | Input voltage range                          | 1IN, 2IN, $\overline{EN}$ | -0.3                         | V <sub>I</sub> + 0.3 | V    |
| V <sub>O</sub>                     | Output voltage                               | 1OUT, 2OUT                |                              | 7                    | V    |
|                                    |                                              | $\overline{RESET}$        |                              | 16.5                 |      |
| Peak output current                |                                              |                           | Internally limited           |                      |      |
| HBM                                | ESD rating                                   |                           |                              | 2                    | kV   |
| Continuous total power dissipation |                                              |                           | See Dissipation Rating Table |                      |      |
| T <sub>J</sub>                     | Operating virtual junction temperature range |                           | -55                          | 150                  | °C   |
| T <sub>stg</sub>                   | Storage temperature range                    |                           | -65                          | 150                  | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## DISSIPATION RATING TABLE

| PACKAGE            | AIR FLOW (CFM) | T <sub>A</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|--------------------|----------------|---------------------------------------|------------------------------------------------|---------------------------------------|---------------------------------------|
| PWP <sup>(1)</sup> | 0              | 3.58 W                                | 3.58 mW/°C                                     | 1.97 W                                | 1.43 W                                |
|                    | 250            | 5.07 W                                | 5.07 mW/°C                                     | 2.79 W                                | 2.03 W                                |

- (1) This parameter is measured with the recommended copper heat-sink pattern on a four-layer PCB, 1-oz copper on 4-in × 4-in ground layer. For more information, refer to TI technical brief literature number SLMA002.

## Recommended Operating Conditions

|                |                                            |            | MIN | MAX | UNIT |
|----------------|--------------------------------------------|------------|-----|-----|------|
| V <sub>I</sub> | Input voltage <sup>(1)</sup>               | 1IN, 2IN   | 2.7 | 10  | V    |
| I <sub>O</sub> | Output current for each LDO <sup>(2)</sup> |            | 0   | 1   | A    |
| V <sub>O</sub> | Output voltage range                       | 1OUT, 2OUT | 1.5 | 5.5 | V    |
| T <sub>J</sub> | Operating virtual junction temperature     |            | -55 | 125 | °C   |

- (1) To calculate the minimum input voltage for maximum output current, use the following equation:  

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$
- (2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

# TPS767D301-EP DUAL-OUTPUT LOW-DROPOUT LINEAR REGULATOR

SGLS327–FEBRUARY 2006

## Electrical Characteristics

$V_i = V_{O(nom)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{EN} = 0$ ,  $C_O = 10\text{ }\mu\text{F}$  (unless otherwise noted)

| PARAMETER                                                      |                                                                  | TEST CONDITIONS                                                                                                                 |                                                                                           | MIN                                                 | TYP       | MAX                        | UNIT          |
|----------------------------------------------------------------|------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------|-----------|----------------------------|---------------|
| $V_O$                                                          | Output voltage <sup>(1)</sup>                                    | Adjustable                                                                                                                      | $1.5\text{ V} \leq V_O \leq 5.5\text{ V}$ ,<br>$10\text{ }\mu\text{A} < I_O < 1\text{ A}$ | $T_J = 25^\circ\text{C}$                            | $V_O$     |                            | V             |
|                                                                |                                                                  |                                                                                                                                 |                                                                                           | $T_J = -55^\circ\text{C}$ to<br>$125^\circ\text{C}$ | $0.97V_O$ | $1.02V_O$                  |               |
|                                                                | 3.3-V output                                                     | $4.3\text{ V} < V_i < 10\text{ V}$ ,<br>$10\text{ }\mu\text{A} < I_O < 1\text{ A}$                                              | $T_J = 25^\circ\text{C}$                                                                  | 3.3                                                 |           |                            |               |
|                                                                |                                                                  |                                                                                                                                 | $T_J = -55^\circ\text{C}$ to<br>$125^\circ\text{C}$                                       | 3.201                                               | 3.366     |                            |               |
| Quiescent current (GND current)<br>for each LDO <sup>(1)</sup> |                                                                  | $10\text{ }\mu\text{A} < I_O < 1\text{ A}$ , $T_J = 25^\circ\text{C}$                                                           |                                                                                           | 85                                                  |           | $\mu\text{A}$              |               |
|                                                                |                                                                  | $I_O = 1\text{ A}$ , $T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$                                                           |                                                                                           | 125                                                 |           |                            |               |
| $\Delta V_O/V_O$                                               | Output voltage line regulation<br>for each LDO <sup>(1)(2)</sup> | $V_O + 1\text{ V} < V_i \leq 10\text{ V}$ , $T_J = 25^\circ\text{C}$                                                            |                                                                                           | 0.01                                                |           | %/V                        |               |
| Output noise voltage                                           |                                                                  | BW = 200 Hz to 100 kHz, $V_O = 1.8\text{ V}$ ,<br>$I_C = 1\text{ A}$ , $C_O = 10\text{ }\mu\text{F}$ , $T_J = 25^\circ\text{C}$ |                                                                                           | 55                                                  |           | $\mu\text{V}_{\text{RMS}}$ |               |
| Output current limit for each LDO                              |                                                                  | $V_O = 0\text{ V}$                                                                                                              |                                                                                           | 1.7                                                 | 2         | A                          |               |
| Thermal shutdown junction temperature                          |                                                                  |                                                                                                                                 |                                                                                           | 150                                                 |           | $^\circ\text{C}$           |               |
| Standby current for each LDO                                   |                                                                  | $2.7\text{ V} < V_i < 10\text{ V}$ ,<br>$\overline{EN} = V_i$                                                                   | $T_J = 25^\circ\text{C}$                                                                  | 1                                                   |           | $\mu\text{A}$              |               |
|                                                                |                                                                  |                                                                                                                                 | $T_J = -55^\circ\text{C}$ to<br>$125^\circ\text{C}$                                       | 10                                                  |           |                            |               |
| FB input current                                               | Adjustable                                                       | FB = 1.5                                                                                                                        |                                                                                           | 2                                                   |           | nA                         |               |
| High-level enable input voltage                                |                                                                  |                                                                                                                                 |                                                                                           | 2                                                   |           | V                          |               |
| Low-level enable input voltage                                 |                                                                  |                                                                                                                                 |                                                                                           |                                                     | 0.8       | V                          |               |
| Power-supply ripple rejection <sup>(1)</sup>                   |                                                                  | $f = 1\text{ KHz}$ , $T_J = 25^\circ\text{C}$ , $C_O = 10\text{ }\mu\text{F}$                                                   |                                                                                           | 60                                                  |           | dB                         |               |
| Reset                                                          | Minimum input voltage<br>for valid RESET                         | $I_{O(\text{RESET})} = 300\text{ }\mu\text{A}$                                                                                  |                                                                                           | 1.1                                                 |           | V                          |               |
|                                                                | Trip threshold voltage                                           | $V_O$ decreasing                                                                                                                |                                                                                           | 92                                                  | 98        | %/ $V_O$                   |               |
|                                                                | Hysteresis voltage                                               | Measured at $V_O$                                                                                                               |                                                                                           | 0.5                                                 |           |                            |               |
|                                                                | Output low voltage                                               | $V_i = 2.7\text{ V}$ ,                                                                                                          | $I_{O(\text{RESET})} = 1\text{ mA}$                                                       | 0.15                                                | 0.4       | V                          |               |
|                                                                | Leakage current                                                  | $V_{(\text{RESET})} = 7\text{ V}$                                                                                               |                                                                                           | 1                                                   |           | $\mu\text{A}$              |               |
|                                                                | RESET time-out delay                                             |                                                                                                                                 |                                                                                           | 200                                                 |           | mV                         |               |
| Input current                                                  | $\overline{EN}$                                                  | $\overline{EN} = 0\text{ V}$                                                                                                    |                                                                                           | -1                                                  | 0         | 1                          | $\mu\text{A}$ |
|                                                                |                                                                  | $\overline{EN} = V_i$                                                                                                           |                                                                                           | -1                                                  |           | 1                          |               |
| Load regulation                                                |                                                                  |                                                                                                                                 |                                                                                           | 3                                                   |           | mV                         |               |
| Dropout voltage <sup>(3)</sup>                                 |                                                                  | $V_O = 3.3\text{ V}$ , $I_O = 1\text{ A}$                                                                                       | $T_J = 25^\circ\text{C}$                                                                  | 350                                                 |           | mV                         |               |
|                                                                |                                                                  |                                                                                                                                 | $T_J = -55^\circ\text{C}$ to<br>$125^\circ\text{C}$                                       | 575                                                 |           |                            |               |

(1) The minimum IN operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1\text{ V}$ , whichever is greater. The maximum IN voltage is 10 V.

(2) If  $V_O \leq 1.8\text{ V}$  then  $V_{i(\text{min})} = 2.7\text{ V}$ ,  $V_{i(\text{max})} = 10\text{ V}$ :

$$\text{Line regulator (mV)} = (\%/\text{V}) \times \frac{V_O(V_{i(\text{max})} - 2.7\text{ V})}{100} \times 1000$$

If  $V_O \geq 2.5\text{ V}$ , then  $V_{i(\text{min})} = V_O + 1\text{ V}$ , and  $V_{i(\text{max})} = 10\text{ V}$ :

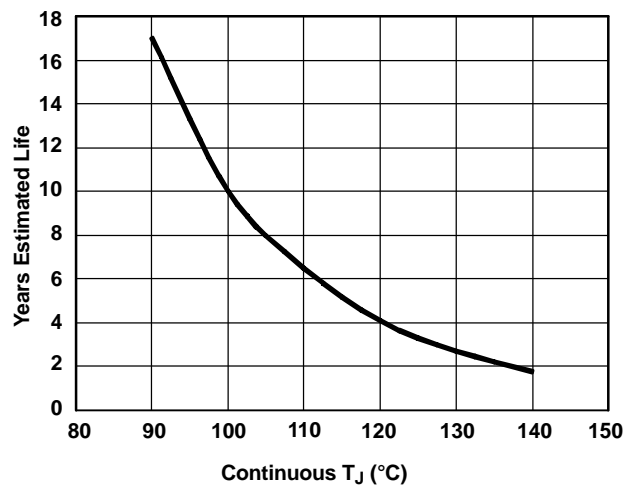
$$\text{Line regulator (mV)} = (\%/\text{V}) \times \frac{V_O[V_{i(\text{max})} - (V_O + 1\text{ V})]}{100} \times 1000$$

(3) IN voltage equals  $V_{O(\text{typ})} - 100\text{ mV}$ ; adjustable output voltage set to 3.3 V nominal with external resistor divider. Dropout voltage of 1.8 V and 2.5 V is limited by input voltage-range limitations.

**TYPICAL CHARACTERISTICS**

**TABLE OF GRAPHS**

|                                    |                                              | <b>FIGURE</b> |
|------------------------------------|----------------------------------------------|---------------|
| Output voltage                     | vs Output current                            | 3, 4, 5       |
|                                    | vs Free-air temperature                      | 6, 7, 8       |
| Ground current                     | vs Free-air temperature                      | 9, 10         |
| Power-supply ripple rejection      | vs Frequency                                 | 11            |
| Output spectral noise density      | vs Frequency                                 | 12            |
| Output impedance                   | vs Frequency                                 | 13            |
| Dropout voltage                    | vs Free-air temperature                      | 14            |
| Line transient response            |                                              | 15, 17        |
| Load transient response            |                                              | 16, 18        |
| Output voltage                     | vs Time                                      | 19            |
| Dropout voltage                    | vs Input voltage                             | 20            |
| Equivalent series resistance (ESR) | vs Output current, $T_A = 25^\circ\text{C}$  | 22            |
|                                    | vs Output current, $T_J = 125^\circ\text{C}$ | 23            |
|                                    | vs Output Current, $T_A = 25^\circ\text{C}$  | 24            |
|                                    | vs Output current, $T_J = 125^\circ\text{C}$ | 25            |



**Figure 2. TPS767D301MPWPREP Estimated Device Life at Elevated Temperatures Wirebond Voiding Fail Mode**

TYPICAL CHARACTERISTICS (continued)

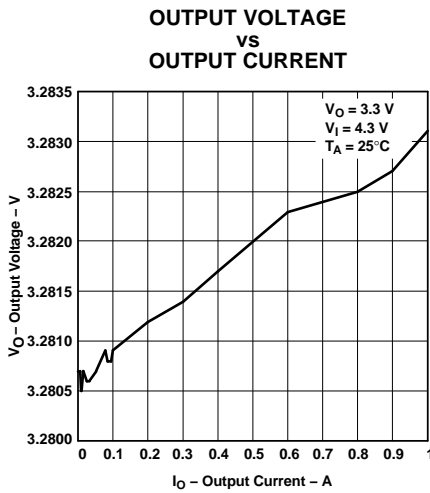


Figure 3.

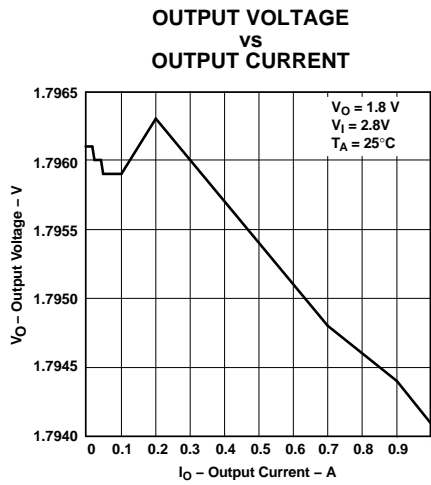


Figure 4.

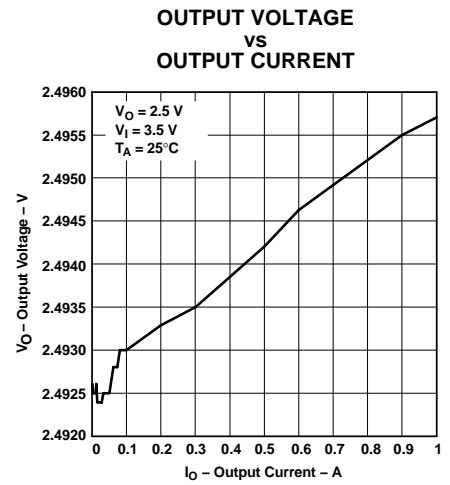


Figure 5.

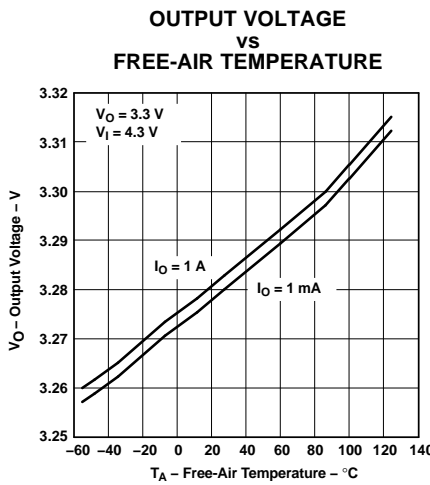


Figure 6.

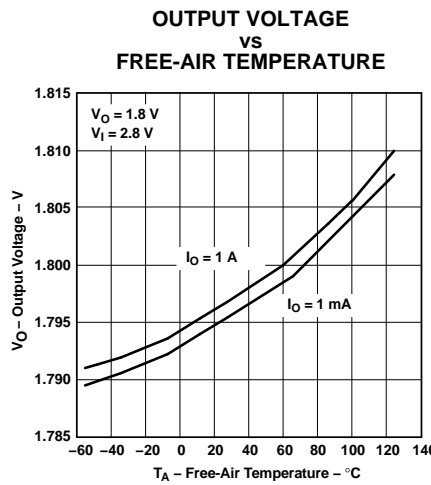


Figure 7.

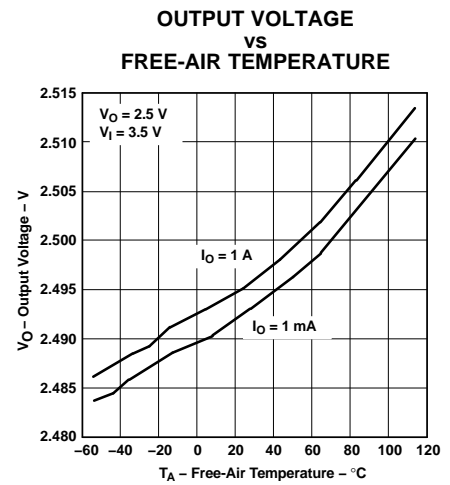


Figure 8.

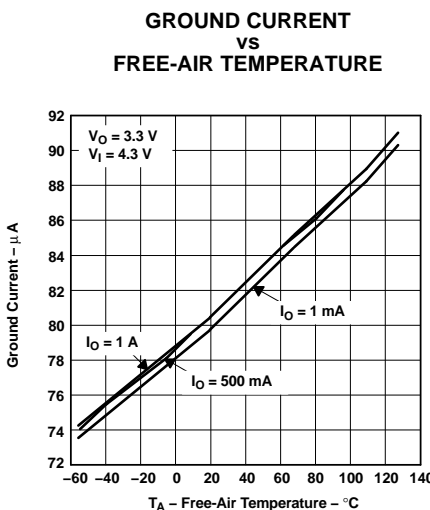


Figure 9.

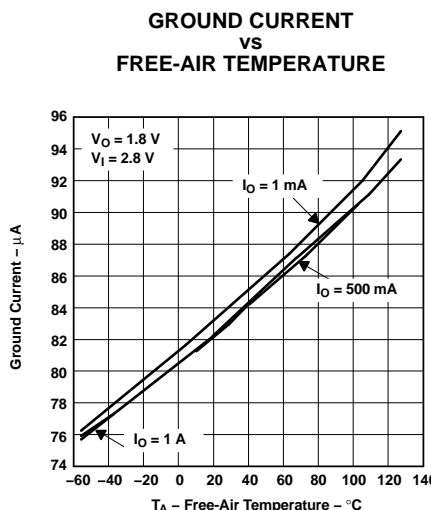


Figure 10.

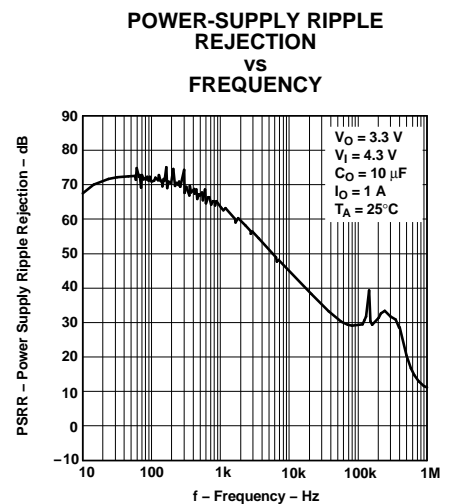


Figure 11.



TYPICAL CHARACTERISTICS (continued) (continued)

OUTPUT SPECTRAL NOISE DENSITY VS FREQUENCY

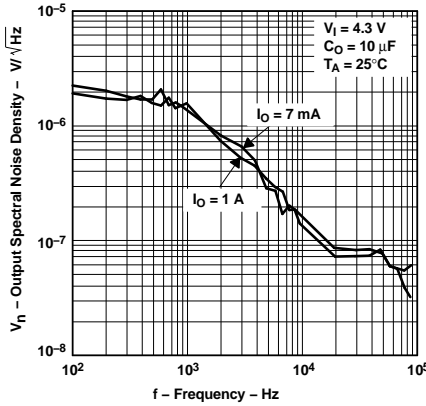


Figure 12.

OUTPUT IMPEDANCE VS FREQUENCY

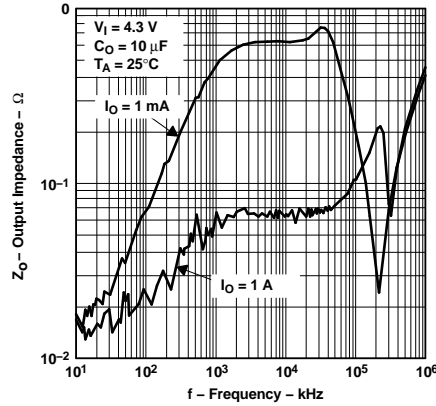


Figure 13.

DROPOUT VOLTAGE VS FREE-AIR TEMPERATURE

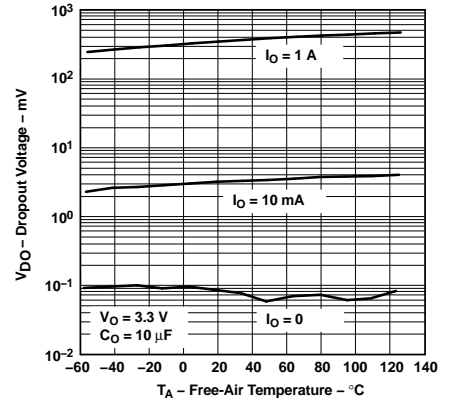


Figure 14.

LINE TRANSIENT RESPONSE

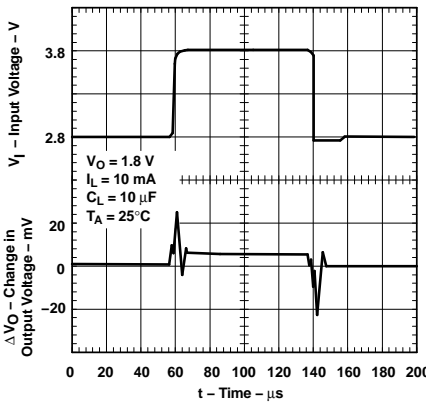


Figure 15.

LOAD TRANSIENT RESPONSE

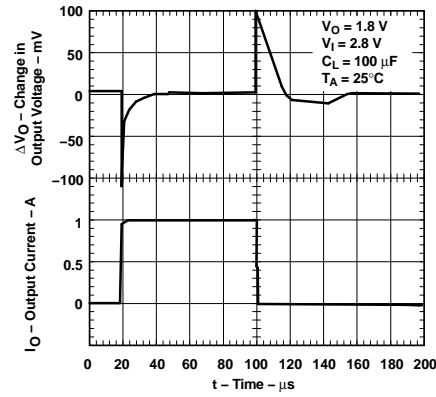


Figure 16.

LINE TRANSIENT RESPONSE

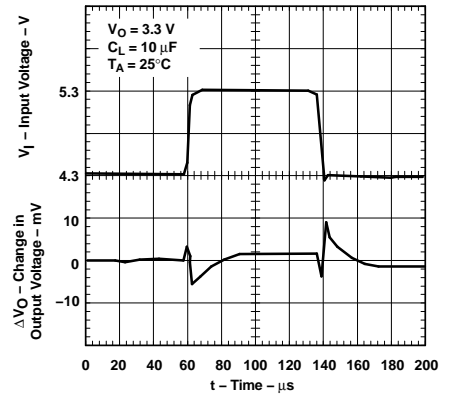


Figure 17.

LOAD TRANSIENT RESPONSE

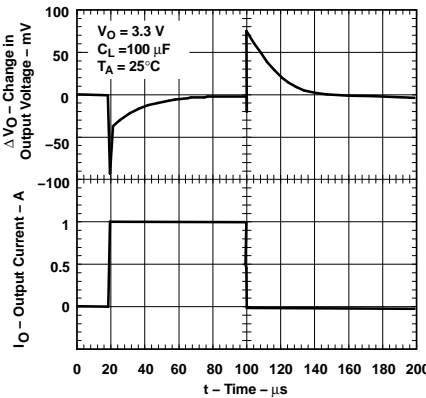


Figure 18.

OUTPUT VOLTAGE VS TIME (AT STARTUP)

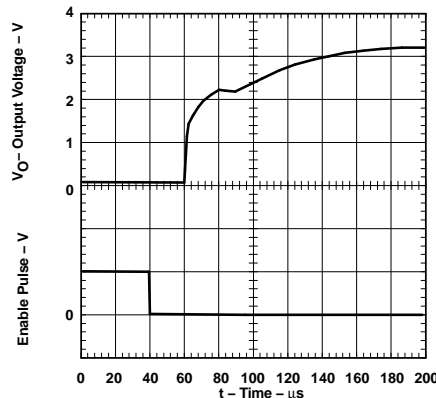


Figure 19.

DROPOUT VOLTAGE VS INPUT VOLTAGE

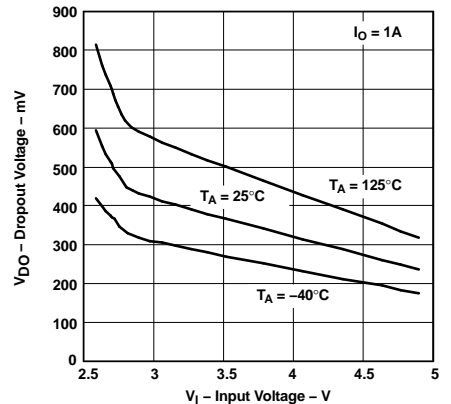


Figure 20.

TYPICAL CHARACTERISTICS (continued) (continued)

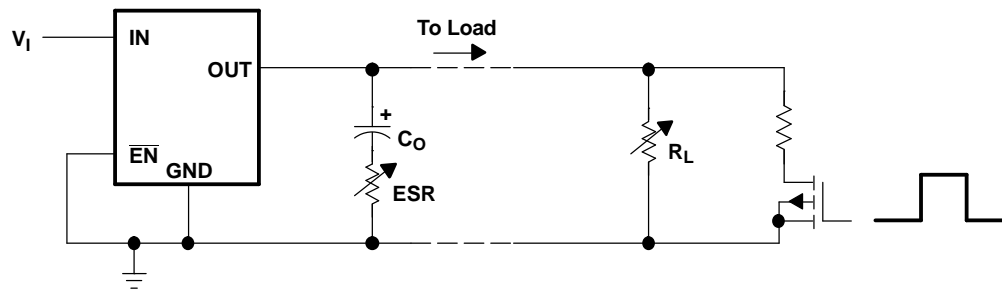


Figure 21. Test Circuit for Typical Regions of Stability  
([Figure 22](#) Through [Figure 25](#)) (Fixed-Output Options)

TYPICAL CHARACTERISTICS (continued)<sup>(1)</sup>

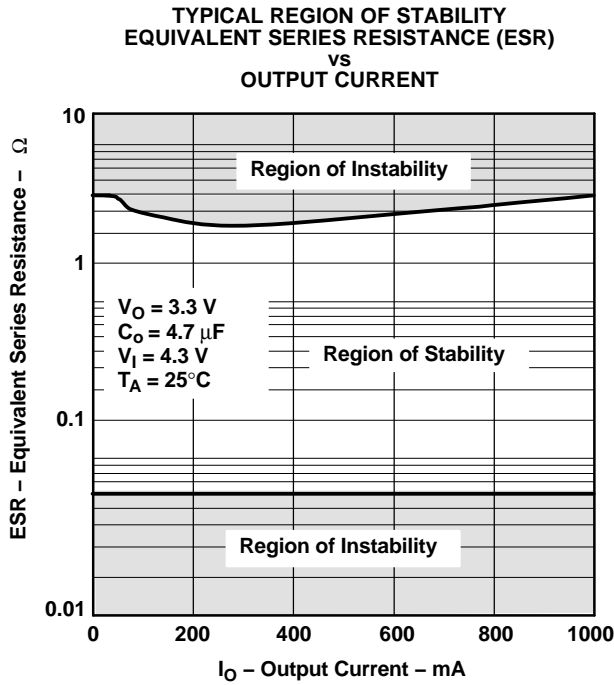


Figure 22.

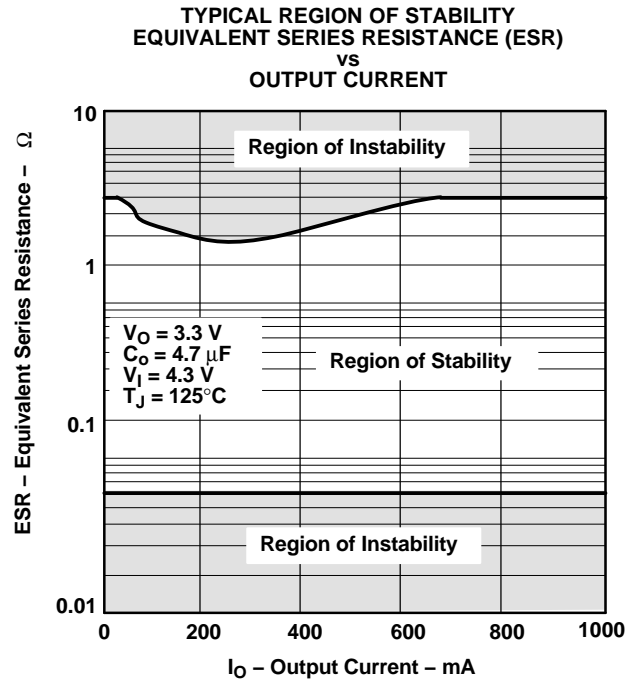


Figure 23.

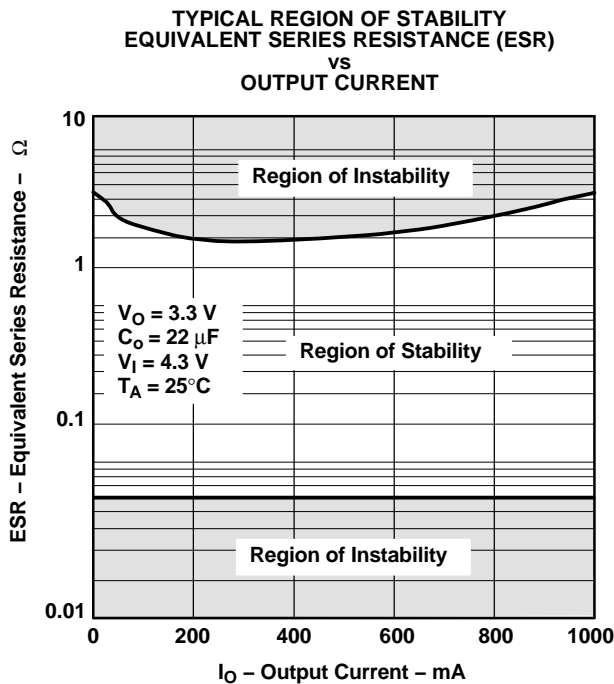


Figure 24.

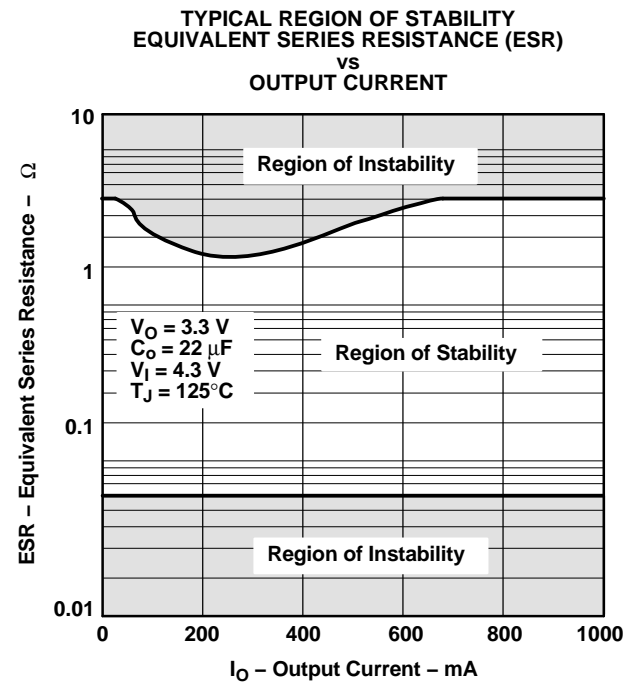


Figure 25.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

## APPLICATION INFORMATION

The features of the TPS767D301-EP (low-dropout voltage, ultra-low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package have enabled the integration of the dual LDO regulator with high output current for use in DSP and other multiple-voltage applications.

### Device Operation

The TPS767D301-EP features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ( $I_B = I_C/\beta$ ). Close examination of the data sheets reveals that these devices typically are specified under near no-load conditions; actual operating currents are much higher, as evidenced by typical quiescent current versus load current curves. The TPS767D301-EP uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range. The TPS767D301-EP specifications reflect actual performance under load conditions.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in  $\beta$  forces an increase in  $I_B$  to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation.

The TPS767D301-EP quiescent current remains low, even when the regulator drops out, eliminating both problems. The TPS767D301-EP also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2  $\mu$ A. If the shutdown feature is not used,  $\overline{EN}$  should be tied to ground. Response to an enable transition is quick; regulated output voltage typically is reestablished in 120  $\mu$ s.

### Minimum Load Requirements

The TPS767D301-EP is stable, even at zero load. No minimum load is required for operation.

### FB – Pin Connection (Adjustable Version Only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop (see [Figure 27](#)). Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier, and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential. In fixed-output options, this pin is a no connect.

### External Capacitor Requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 mF) improves load transient response and noise rejection when the TPS767D301-EP is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767D301-EP requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10  $\mu$ F and the equivalent series resistance (ESR) must be between 60 m $\Omega$  and 1.5  $\Omega$ . Capacitor values of 10  $\mu$ F or larger are acceptable, provided the ESR is less than 1.5  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements previously described.

When it is necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the previous guidelines.

APPLICATION INFORMATION (continued)

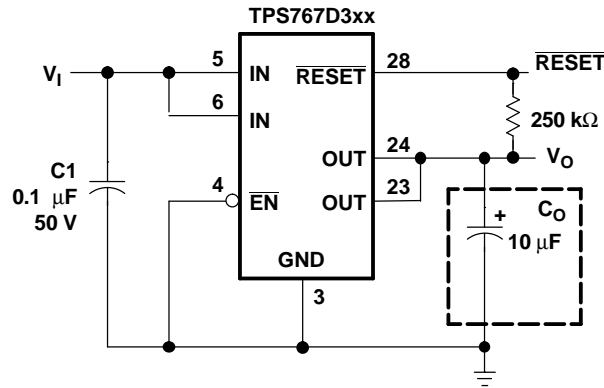


Figure 26. Typical Application Circuit (Fixed Versions) for Single Channel

Programming the TPS767D301-EP Adjustable LDO Regulator

The output voltage of the TPS767D301-EP adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where:

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)} \quad (1)$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower-value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

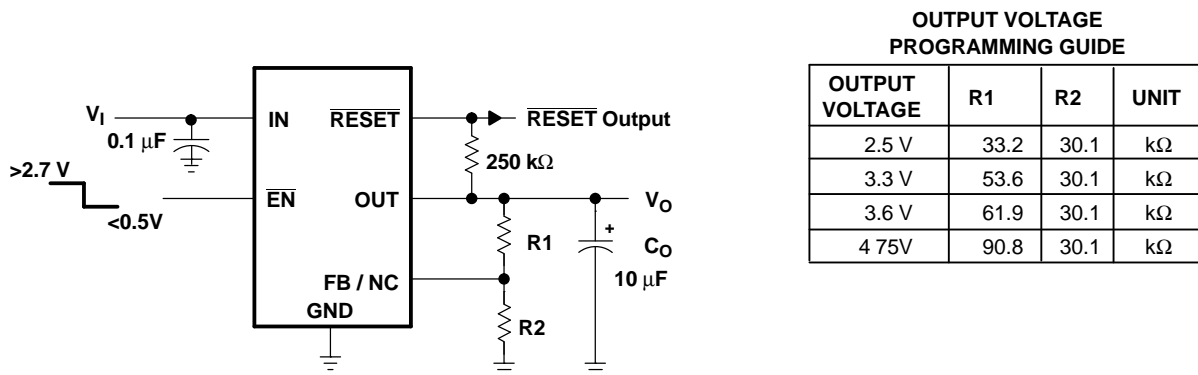


Figure 27. TPS767D301-EP Adjustable LDO Regulator Programming

## APPLICATION INFORMATION (continued)

### Reset Indicator

The TPS767D301-EP features a  $\overline{\text{RESET}}$  output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage. When the output drops to 95% (typical) of its regulated value, the  $\overline{\text{RESET}}$  output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating.  $\overline{\text{RESET}}$  can be used to drive power-on reset circuitry or as a low-battery indicator.

### Regulator Protection

The TPS767D301-EP PMOS-pass transistor has a built-in back-gate diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767D301-EP also features internal current limiting and thermal protection. During normal operation, the TPS767D301-EP limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

### Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(\max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(\max)}$ .

The maximum power dissipation limit is determined using the following equation:

$$P_{D(\max)} = \frac{T_{J\max} - T_A}{R_{\theta JA}}$$

where:

$T_{J\max}$  is the maximum allowable junction temperature

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, i.e., 27.9°C/W for the 28-terminal PWP with no airflow.

$T_A$  is the ambient temperature.

(3)

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

**PACKAGING INFORMATION**

| Orderable Device  | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS767D301MPWPREP | ACTIVE                | HTSSOP       | PWP             | 28   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| V62/06617-01XE    | ACTIVE                | HTSSOP       | PWP             | 28   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF TPS767D301-EP :**

- Catalog: [TPS767D301](#)
- Automotive: [TPS767D301-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS767D301MPWPREP | HTSSOP       | PWP             | 28   | 2000 | 330.0              | 16.4               | 6.9     | 10.2    | 1.8     | 12.0    | 16.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**

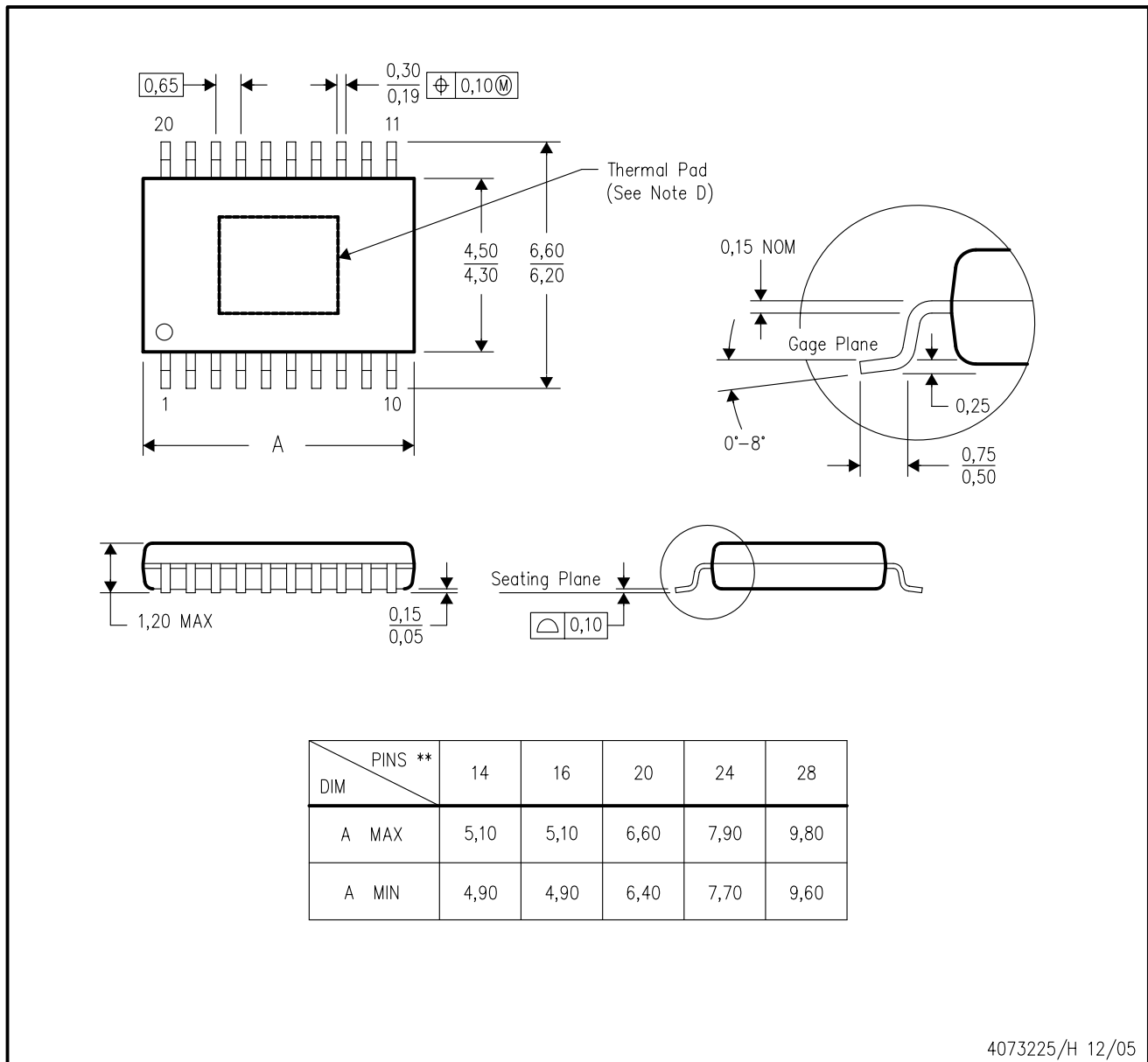


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS767D301MPWPREP | HTSSOP       | PWP             | 28   | 2000 | 346.0       | 346.0      | 33.0        |

PWP (R-PDSO-G\*\*) 20 PIN SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073225/H 12/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MO-153

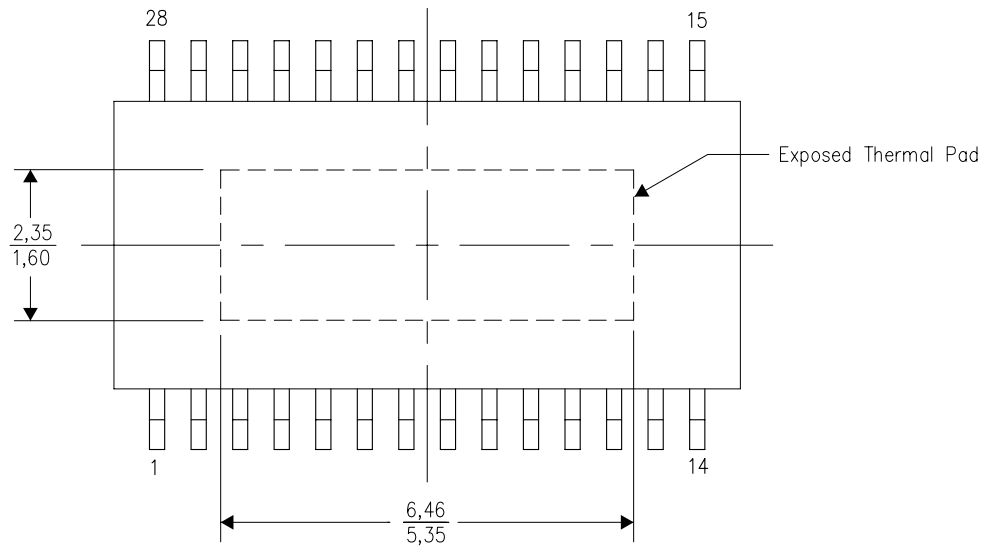
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

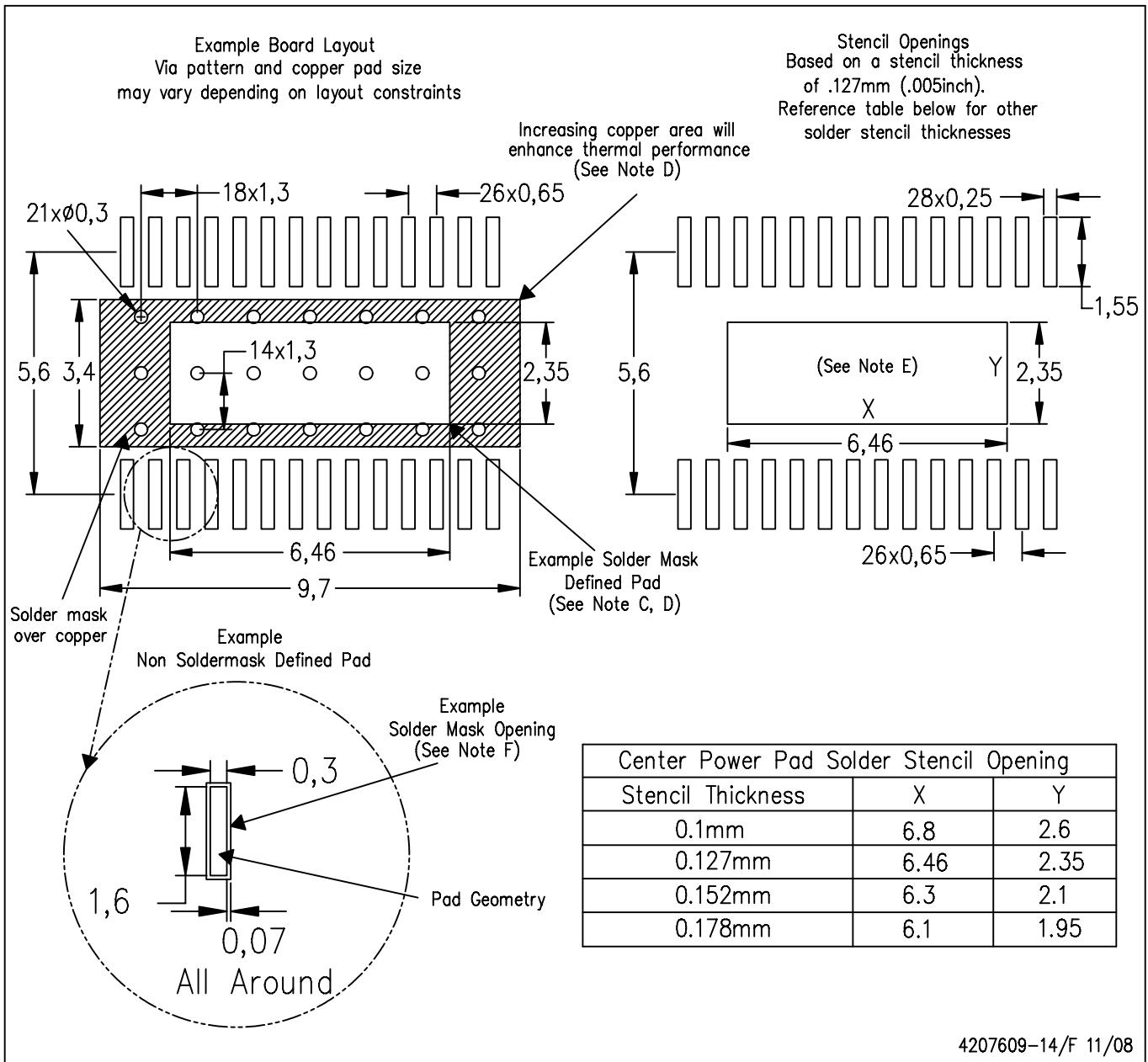


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R-PDSO-G28) PowerPAD™



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- PowerPAD is a trademark of Texas Instruments.

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| DSP                         | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           |
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| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               |

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| Digital Control    | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Medical            | <a href="http://www.ti.com/medical">www.ti.com/medical</a>               |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Optical Networking | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
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